

PWCT

DISPLAY SYSTEM SPECIFICATIONS

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Display System Specifications

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INTRODUCTION

Following is a complete description of the alphanumeric and graphic display system to be provided for the UCB - ARPA project. The display system will be housed in a free-standing cabinet which includes a 21-inch cathode ray tube, digitally controlled line and symbol generation circuitry, and control logic to provide the necessary buffering and control to interconnect the DEC PDP-5 computer and the basic display.

The display system will have a capability for symbol plotting, line drawing, and for formatting symbols in a typewritten-like mode. It will also include a "script mode", wherein short vector descriptions will be used to increment the display as a continuous broken line in a manner capable of reproducing script information.

The equipment will also house and provide the necessary power supplies for the RAND Tablet Logic (the Tablet Logic is provided by UCB). A direct-feedback feature will allow the Tablet coordinates to be displayed directly. A Tablet Comparator circuit in the display system will detect when the total CRT deflection is equal to the tablet coordinates.

Forced air cooling will permit continuous operation in a normal office environment. The system will operate from conventional 110-volt, 60-cycle, single phase lines. All equipment will be furnished in accordance with good commercial practice. Wherever practical, plug-in printed circuit cards and solid state components will be utilized.

Figure I-1 is a simplified system block diagram.

Documentation will be supplied as follows:

1. A brief descriptive write-up of each functional module, including theory of operation and adjustments.
2. Circuit diagrams of all printed circuit cards and wired sub-assemblies.
3. Block and logic diagrams.
4. Parts and recommended spares lists, with sources and substitutes indicated for unusual or special parts.

The console is arranged with only power, variable intensity, and an auxiliary pushbutton available as operator controls. A false panel conceals additional deflection amplifier controls. All other adjustments are screw driver adjustments from the rear.

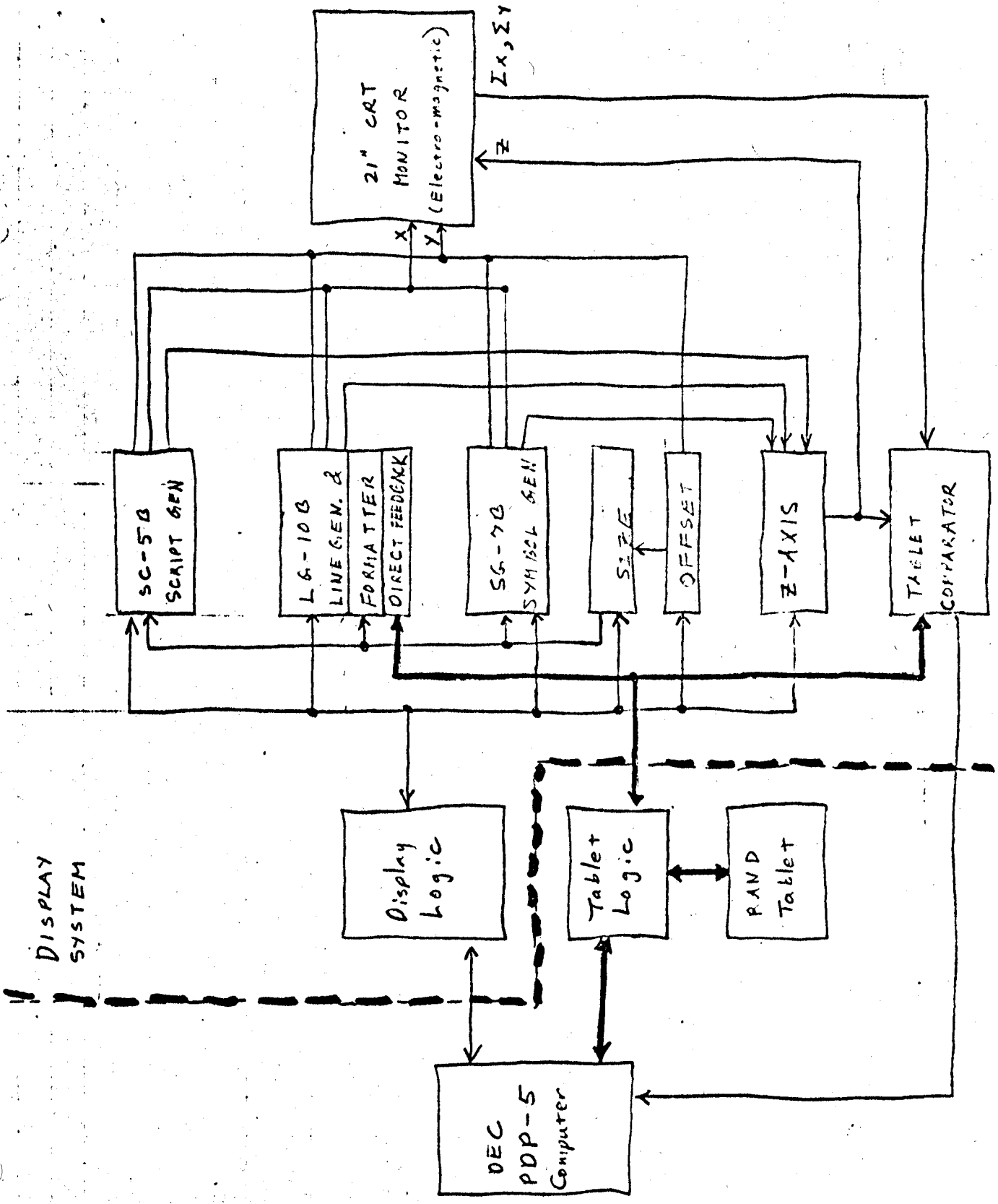


Fig. 1 System block diagram. The portion marked Display System is described in detail.

GENERAL DISPLAY CHARACTERISTICS

The display area will be a 12 x 12-inch square on the face of a 21-inch cathode ray tube. The face plate will be spherical with at least a 33-inch radius of curvature.

There will be 1024 discrete positions along each axis, addressable by natural binary numbers in the order left-to-right for the x-axis, and bottom-to-top for y-axis.

Brightness is controlled by a manual, front panel control plus one of three digitally selectable, manually adjustable internal controls. This allows program selection of one of three preset brightness levels. These three levels are defined as DIM, NORMAL, and BRITE.

At the NORMAL programmed brightness setting, automatic internal brightness compensation maintains constant intensity for:

- a. Lines ranging from 10 units long to 1000 units long.
- b. Symbols within the 2:1 range of 128 symbols/line to 64 line.
- c. Script over the full 4:1 size range.

At maximum allowable CRT brightness there is a considerable increase in beam diameter. The exact performance of the display when programmed for "BRITE" display, will depend on how closely this maximum brightness is approached.

Non linearities in the CRT brightness control elements cause similar deviations in the programmed "DIM" mode. In this case brightness compensation may not be fully attainable over the ranges specified above. The equipment is designed, however, with 10 independent full range brightness compensation adjustments for the various symbol and script sizes, line generator ranges, and programmed levels. This will allow minimization of the above limitations within the capabilities of the specific CRT and phosphor used.

At a refresh rate of 30 frames per second, the three intensity levels may be set such that they are distinguishable regardless of the size of lines or symbols and still allow comfortable viewing at 2 ft. in 10 ft. candles of vertically incident ambient from a diffused incandescent source.

At any place on the 12" by 12" viewing area the beam or spot diameter will not exceed 25 mils in width at NORMAL brightness setting. The edge of the beam is defined as that point where the intensity is 60% below the center intensity. At NORMAL brightness the display will be capable of resolving 128 well formed characters across the display area in the least favorable y-position.

The CRT phosphor will be P4.

The deflection system is magnetic and uses all solid state components. Worst case jump settle time is less than 30 μ seconds.

Axial non-linearity will not exceed 1% of full scale measured over arbitrary 100 raster point lengths along either axis.

Total instantaneous placement error of the displayed objects due to all causes will be less than \pm one raster point per cycle (approx. 30 ms.). The total accumulative displacement is not to exceed \pm 3 raster points.

SYMBOL GENERATOR

The standard Model SG7B symbol generator, as described in Appendix B, Proposal 665-C (see Appendix B) will be provided. This will allow the set of 128 symbols described in Figure 2 and Appendix C. The symbols are selected by Symbol Words from the PDP-5. Each Symbol Word also contains one bit to select the brightness and three bits to select the y-offset and size of each symbol. The total time required to select any symbol, produce it on the CRT, and increment the format registers if in the format mode will be less than twelve μ sec.

Four different, manually adjustable and digitally selected symbol sizes will be provided. The minimum size will be commensurate with 128 symbols per 12" line; maximum size will be four times minimum. The sizes will initially be adjusted to allow formatting of 128 and 85 symbols per line. Symbol size adjustments will be with respect to a fixed point at the symbol origin (near the lower left corner of the symbol). The aspect ratio for each size is independently adjustable within the overall size range.

Dynamic range of the symbol generator will allow generation of normal-size designated symbols which will extend a total of two normal block spaces either, or both, horizontally or vertically. The symbol generator integrators will necessarily be required to integrate both positive and negative as is clear from symbol placement relative to specified origin (See Appendix C).

Figure 2a UCB SYMBOLS

(Detailed drawings of all symbols are in Appendix C)

<u>Octal Code</u>	<u>Symbol</u>	<u>Octal Code</u>	<u>Symbol</u>
000	⊙ (centered circle)	100	⊙
001	a	101	A
002	b	102	B
003	c	103	C
004	d	104	D
005	e	105	E
006	f	106	F
007	g	107	G
010	h	110	H
011	i	111	I
012	j	112	J
013	k	113	K
014	l	114	L
015	m	115	M
016	n	116	N
017	o	117	O
020	p	120	P
021	q	121	Q
022	r	122	R
023	s	123	S
024	t	124	T
025	u	125	U
026	v	126	V
027	w	127	W
030	x	130	X
031	y	131	Y
032	z	132	Z
033	⌈	133	[
034	⌊	134	(vertical)
035	⌋	135]
036	⌆	136	↑
037	⌇	137	→

Figure 2b UCB SYMBOLS

<u>Octal Code</u>	<u>Symbol</u>	<u>Octal Code</u>	<u>Symbol</u>	
040	⊙	140	(blank)	
041	⊙	141	⋮	
042	⊙	142	⋮	
043	⊙	143	#	
044	⊙	144	\$	
045	⊙	145	%	
046	⊙	146	&	
047	⊙	147	'	
050	⊙	150	(
051	⊙	151)	
052	⊙	152	*	
053	⊙	153	+	
054	⊙	154	'	(prime)
055	⊙	155	-	(minus)
056	⊙	156	.	(period)
057	⊙	157	/	
060	⊙	160	0	
061	⊙	161	1	
062	⊙	162	2	
063	√	163	3	
064	∑	164	4	
065	∫	165	5	
066	∏	166	6	
067	—	167	7	(horizontal)
070	•	170	8	(multiply dot)
071	↑	171	9	
072	↓	172	:	
073	▲	173	;	
074	▶	174	<	
075	◀	175	=	
076	▼	176	>	
077	×	177	?	(centered cross)

LINE GENERATOR

The standard MODEL IG.-10B line generator is described in Appendix A, proposal 665-C (see Appendix A) will be provided. The line generator is used to produce the analog signals required to deflect the CRT beam linearly between any two specified points on the display. Each point of x, y coordinates, 10-bits each, will specify the terminal point of a line to be drawn from the current value of the line generator registers (called "initial point"). When the line is completed, the terminal point becomes the initial point for the next line.

Four types of lines are provided - position only, position with terminal point intensified, segmented line, and solid line. As mentioned above, three different brightness levels are available for lines.

Dashed lines along either axis will have dash segments of $1/8$ " \pm $1/16$ ". Diagonal lines will have dash segments approximately 1.4 times longer. Both end points will be intensified.

The longest length lines will be drawn in $175 \mu\text{sec.}$ or less.

Lines will be drawn at a constant writing rate over line lengths of 40:1. Generated lines will not deviate from an ideal line by more than 1% of the line length or 2 raster points, whichever is greater. Angular deviation will not exceed 5° at any point on the line.

FORMATTED SYMBOLS

One mode of operation of the display is the "format mode" in which successive symbols are drawn in typewritten-like fashion. The first symbol in a formatted string is drawn at the current value specified by the line generation accumulators (plus any y-offset). At the completion of each symbol, the x-accumulator is incremented by an amount proportional to the previous (i.e., current) symbol size. One or two sequential pulses to the format counter (x-accumulator) will accomplish the spacing. The choice of these increment sizes is set in the hardware; the following possibilities will exist:

First Pulse to Stage	2^4	2^3	
Second Pulse Open	64	128	Characters per line
Second Pulse to Stage 2^2	--	85	
Second Pulse to Stage 2^3	42	--	

The initial setting (circled) will correspond to the "small" and "normal" size symbols as specified in the section OFFSET SYMBOLS. Upon a "line-feed" command, the y-accumulator is decremented by one of three amounts as follows:

<u>Command</u>	<u>Increment Pulse to Stage</u>
Line-feed $\frac{1}{2}$	2^4
Line-feed 1	2^5
Line-feed 2	2^6

Other format commands provide for storing two values of the x-accumulator in the hardware to provide two tab or margin settings. These margin settings will be lost each time the format mode is left. The x-accumulator can be restored to either of these two margins upon command. An overflow of the x-accumulator will cause an automatic "Return to primary margin and line-feed 1" command when in the format mode.

In the format mode, vertical and horizontal placement of characters will be better than \pm one raster point relative to plot mode points at character origins.

OFFSET SYMBOLS

As stated above, three bits of each Symbol Word from the PDP-5 specify 1 of 8 offsets in the y-direction, and 1 of 4 sizes. The amount of offset is directly proportional to the three-bit binary code as shown below, i.e., the positions are equally spaced in y (unit spacing).

Position	Initial Symbol Size	Implied Size Code	Offset Code
7	small	00	111
6	normal	01	110
5	small	00	101
4	normal/small	01/00	000/100
3	small	00	011
2	normal	01	010
1	small	00	001

A manual adjustment is provided for the unit spacing; the initial unit spacing will be $8/1024$ of full screen. The unit spacing is adjustable over a range of 4 raster points to 20 raster points.

Although only two of the symbol sizes are used in this initial setting, four are provided in the hardware.

This facility is used for placing the formatted symbols in one of several subscript or superscript positions.

SCRIPT GENERATOR

The script generator generates any one of 25 line segments shown on page 4 of the Burroughs Symbol Generators description (Appendix B). These segments are specified by five-bit numbers from 0 to 24 (called strokes). Upon entering the script mode, one of two brightness levels (the same as for symbols), one of 4 sizes, and one of 8 offsets (the same as for symbols) are specified for all the following strokes. Notice here that the size is independent of the offset code as is not the case in the format mode.

In a PDP-5 Script Word, two 5-bit strokes and one z-axis bit are specified. When the z-axis bit is high, both strokes are to be drawn blanked. Otherwise, both strokes are drawn unblanked.

Of the 32 combinations in the 5-bit stroke code, 5 control codes will allow flexible control of resetting of the integrators and will provide 128 and 85-symbol per line spacing for application of the script generator to generate special symbols. See Figure 5.

The script generator will be capable of drawing segments at intervals less than 2.0 μ sec including setup, but asynchronously. The script integrators will hold any value up to full screen deflection for 33 ms with less than 1 $\frac{1}{2}$ % change during the interval.

The dynamic range of the output integrators is ± 256 units in each axis. The total reset time for these integrators will be less than 10 μ sec.

The four logically addressable segment sizes will be manually adjustable over a maximum range of 1:4. At maximum setting, ± 256 unit steps causes \pm full screen deflection; at minimum setting, ± 256 unit steps causes $\pm \frac{1}{4}$ screen deflection in each axis. The initial settings will be as follows:

<u>Size Code</u>	<u>Length of Short Stroke</u> (#units on 1024 grid)
00	1
01	2
10	3
11	4

TABLET COMPARATOR

The comparator accepts 10-bits x and 10-bits y, 1-bit validity from the Tablet, one total-analog-x* and one total-analog-y* from the monitor and z-axis blank/unblank. The output is a 1- μ sec pulse when the pen and unblanked beam positions match. This pulse will set a "Match" toggle, if the toggle is enabled (by an enable bit in PDP-5 Control Words), which will subsequently cause a PDP-5 interrupt. At the same time, the display is temporarily halted until the Display Address Register is read by the PDP-5. Anytime a match causes a PDP-5 interrupt, the address of the word** in the PDP-5 memory whose display caused the match is equal to the contents of the Display Address Register minus one.

* Weighted sum of all analog signals which are causing beam deflection during unblank, i.e., a signal proportional to beam position.

** This will be a Symbol Word if a symbol, a Script Word if in Script Mode, a y-Word if a line caused the match.

A Match will never occur during a direct-feedback cycle. Also a match will inhibit further matches in the current frame time. Hence, three Match toggles will be necessary. One toggle (called Match Enabled) in flowcharts remembers bit II of Change Mode Control Words. The second (called MAT 1 in flowcharts) causes the PDP-5 interrupt and is reset by a PDP-5 pulse. The third (called MAT 2) remembers that a match has occurred in a given frame and, therefore, allows only one match per frame.

Provision will be made for an adjustable O.K. band between the tablet value and deflection signal. This band should be adjustable from $\frac{1}{2}\%$ to 2% of full screen deflection.

DIRECT FEEDBACK

At approximately each 5 ms the normal display functions will be interrupted at a convenient point in time and an externally generated set of x, y-coordinates switched into the D/A converters to display a point. This information is held in the RAND Tablet Logic. A control line from the Tablet Logic will indicate that the Tablet coordinates may be read to cause a direct-feedback cycle. This signal will also anticipate the Tablet coordinate "non-valid" condition. The 5-ms clock is part of the Tablet Logic.

DISPLAY GO BUTTON

In order to start the display, a special "GO" button will be provided on the front of the console. Whenever this button is depressed, a pulse is generated which sets a "GO" toggle. Whenever the "GO" toggle is set, the display stops reading data from the PDP-5 and prepares to execute an Indirect Address Read Cycle. The Display Address Register (DAR) will be reset to a "wired" address; location 3 in the initial setting. Since the Indirect Address toggle is on, the number at location 3 represents the location of the first display command. A PDP-5 IOT pulse will initiate the Read Cycle*.

This "GO" button may be depressed at any time and is an emergency type operation, hence no data currently in the display registers, with the exception of the above mentioned, need be preserved. Generally, this button will be depressed when the display is first turned on, or when the operator has lost control of his display program. "GO" also starts Frame Timer.

DISPLAY CONTROL LOGIC

The logical control to drive the symbol, line, and script generators is derived from 12-bit PDP-5 words. These words are accessed from the PDP-5 using the Data Break system of I/O. The display logic supplies the memory address for each display word; display words are taken from consecutive core locations until a Jump type control word is read, in which case the addressing scheme is identical to that in the PDP-5, including the page and indirect address bits.

* Figure 8, PDP-5 To Display Logic, Item (4).

In order to achieve maximum efficiency from the PDP-5, a buffer register is part of the Display Logic. The buffer will usually contain the next Display Word before the Basic Display components are finished with the previous word. This is achieved by only dropping the PDP-5 Break Request line if the basic display is busy at the time the present word is being read from the PDP-5.

From the PDP-5 will come a pulse to signify that an address has been accepted, and 3 or more* μ sec later another pulse to be used to read the PDP-5 memory buffer. The Address Accepted pulse may be used to clear the display buffer register, but is probably otherwise unnecessary.

There are three general classes of PDP-5 Display Words; Control Words, Data Words, and Indirect Address Words. Control Words are distinguishable from Data Words by PDP-5 bit-0. Three of the four control words cause a new address to be read into the Display address Register, among these is a deferred or Indirect Address Word. Note that Indirect Address Words can always be stored in locations in the PDP-5 so that they never interfere with distinguishing Data Words from Control Words.

The three transfer control words operate as follows:

IUT - Immediate Unconditional Transfer

An immediate transfer takes place. Since there is no way to prevent an IUT program loop that displays a single line or symbol only, an Intensity control must appear on the console with the Power and Go buttons.

FUT - Frame Unconditional Transfer

A transfer takes place when the (~ 30 ms) Frame Timer has elapsed. If a FUT is detected before Frame Timer elapse (End of Frame), the display will remain static (hang-up) but not hang-up PDP-5 until End of Frame and then continue with the transfer. In all cases, the Frame Timer is started** by the FUT transfer. The Frame Timer is part of the Display Logic and is necessary to insure a Frame Time no shorter than its elapsed time (~ 30 ms) given that at least one FUT will occur in each PDP-5 display buffer sequence.

MCT - Match Conditional Transfer

MCT is the same as a FUT except that MCT will transfer only if a match has occurred in the current frame. Otherwise, the MCT is ignored. MCT must depend on the Frame Timer, and also restart the Frame Timer, to help prevent burn-up of the phosphor if the MCT is used to cause display of the symbol or line that caused the match.

* This is because the I/O Halt facility of the PDP-5 is being used; hence, the PDP-5 may halt just after the Address Accepted pulse is generated.

** The Frame Timer is also started by the GO button.

The fourth type of control word is the Change Mode Word in which one of four possible modes is selected; (a) Random Character, (b) Line, (c) Format, and (d) Script. The Change Mode words, besides specifying a new mode, give information that applies to all data until the next Change Mode word, such as line type and brightness, match enable, script size and offset, etc. (see Figure 3).

In the Random Character Mode, successive groups of 3 words are data words in this order: x-Word, y-Word, Symbol Word. First the line to x, y is drawn, then the symbol at location x, y. No incrementing of the format counters occurs in this mode.

In the Line Mode, successive groups of 2 words are data words in this order: x-Word, y-Word. A line is drawn to x, y.

In the Format Mode, every word is a Symbol Word which selects a symbol, y-offset (which implies a symbol size) and a brightness level. After each symbol is drawn, the appropriate levels of the format counters are incremented.

In the Script Mode, every word contains 2 stroke codes, and a z-axis bit. The strokes are accumulated by a tail-on-head fashion similar to the lines. Some of the stroke codes specify control operations.

The carriage-return like functions are initiated by decoding 3 bits in the Change Format words. Bit-11 of every Change Mode word sets or resets the Match Enable Toggle. Bits in the Random Character and Line Mode Control words specify the 3 line brightnesses and 4 line types. Bits in the Script Mode Control word select the size, offset, and brightness of the strokes.

Figures 3, 4, and 5 give a detailed description of the PDP-5 word formats.

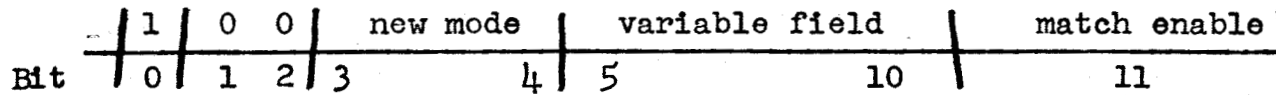
CONTROL WORD FORMATS

	1 bit data/ control	control code	2 bits mode code or indirect & page address		variable field		
bits	0	.1	2	3	4	5	11

All control words, bit 0 1

Control Code		Bits	4	5	11
CDM	00 Change Display Mode	new mode code (see next page)		see next page	
IUT	01 Immediate Unconditional Transfer	direct/ indirect	memory page	7-bit address within "page"	
FUT	10 Frame Unconditional Transfer	direct/ indirect	memory page	7-bit address within "page"	
MUT	11 Match Conditional Transfer (Transfers only if a Match in current frame and Frame Timer has elapsed)	direct/ indirect	memory page	7-bit address within "page"	

Figure 4a MODE CONTROL FORMAT



bits 3,4
New Mode code

New Mode code	Variable field bits					
	5	6	7	8	9	10
00 .. Random Character	line type		brightness		unused	
	00..Jump		Lines	Chars		
	01..Dot		00..Normal	Normal		
	10..Dash		01..Bright	Bright		
	11..Solid		10..Dim	Normal		
			11..Dim	Bright		
01 .. Line	line type		brightness		unused	
	00..Jump		00..Normal			
	01..Dot		01..Bright			
	10..Dash		10..Dim			
	11..Solid		11..Dim			

New Mode code	5 6 7			8 9 10		
	10 .. Format	000	001	010	unused	
	100	101	110			
	011	111				

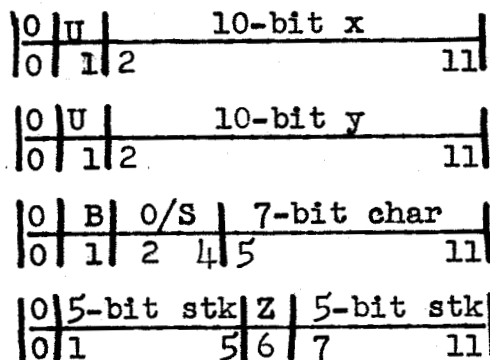
Figure 4b MODE CONTROL FORMAT

bits 3,4 <u>New Mode Code</u>	Variable field bits				size 00..small 01..normal 10..medium 11..large
	5	6	7	8	
11 .. Script	brightness 0..Normal 1..Bright		offset see OFFSET SYMBOLS above		

Match enable--bit 11

- 0..disable matches
- 1..enable matches

Figure 5 DATA WORD FORMATS



Used for random characters and lines

Used for random characters and lines

Used for random and formatted characters

Used for script mode

B = brightness
 0--normal
 1--bright

O/S = offset/size
 see OFFSET SYMBOLS above

7-bit char = 7-bit character
 see Fig. 2 above

Z = z-axis control
 0--unblank
 1--blank

U = unused

5-bit stroke codes

$0_{10} - 24_{10}$.. specify possible script generator strokes. 0_{10} is null stroke

25_{10} .. reset x integrator

26_{10} .. reset y integrator

27_{10} .. reset both x and y integrator

28_{10} .. increment x gross position register by 8 units and reset both x and y integrator

29_{10} .. increment x gross position register by 12 units and reset both x and y integrator

CONTROL LOGIC FLOW CHART

The following is believed to be an acceptable flow chart representing the Display Control logic. However, there may be equivalent flow-charts which perform the same functions but are logically simpler in terms of the hardware implementation. If inconsistencies or questions arise, the preceding text should be considered as valid.

LOGIC FLOW CHART CODES

MCT - Match Conditional Transfer
FCT - 30 ms Cycle Conditional Transfer
IUT - Unconditional Transfer
AR - Address Register, 12 bit
IB - Input Buffer, 12 bit
Ind - Indirect Address
WC - Word Counter
MB - PDP-5 Memory Buffer
MAT 2 - Match ff 2, allows only one match/frame
MAT 1 - Match ff 1, causes PDP-5 interrupt
EOF - End of Frame, 30-ms Frame Timer

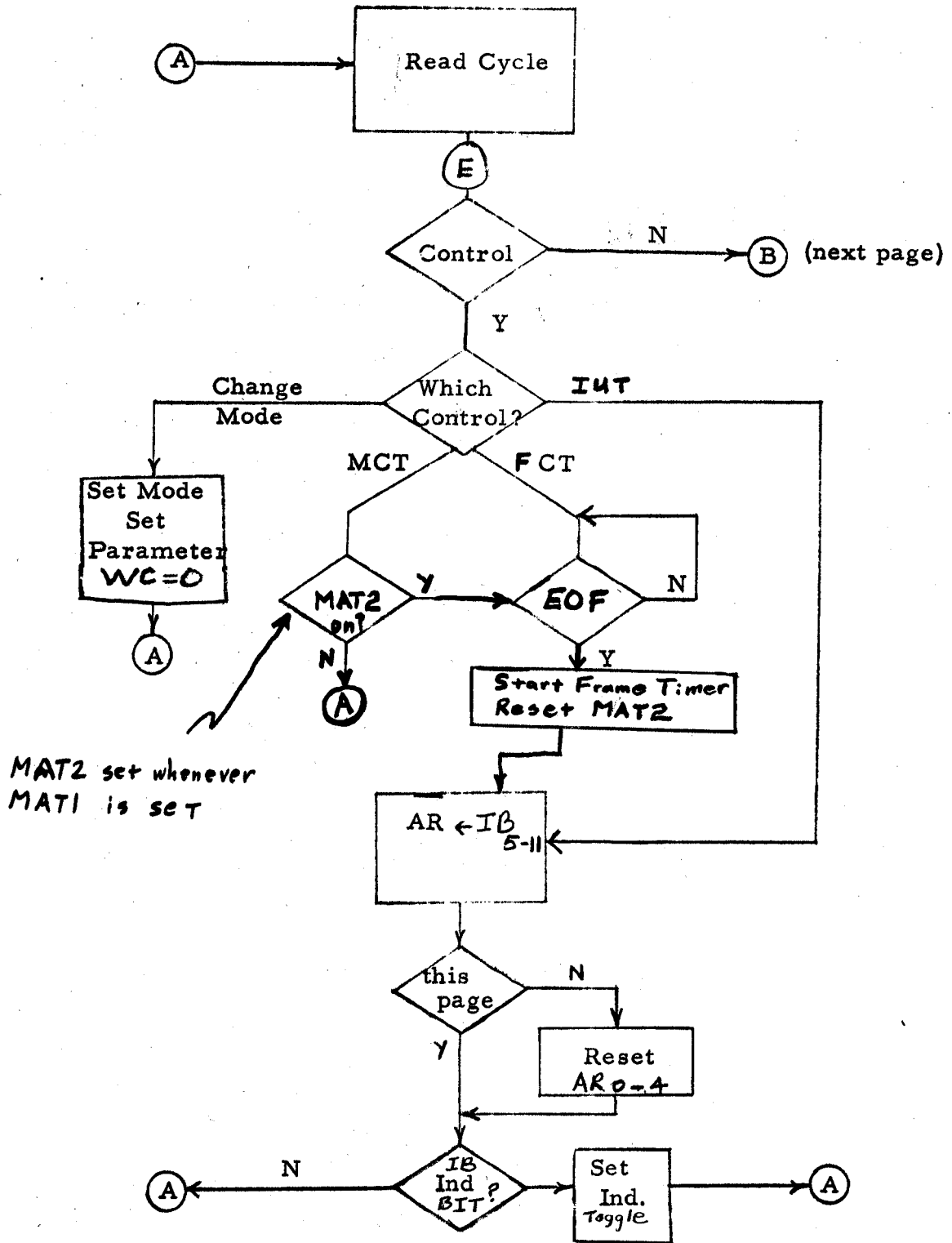


Fig. 7a

SYSTEM FLOW CHART

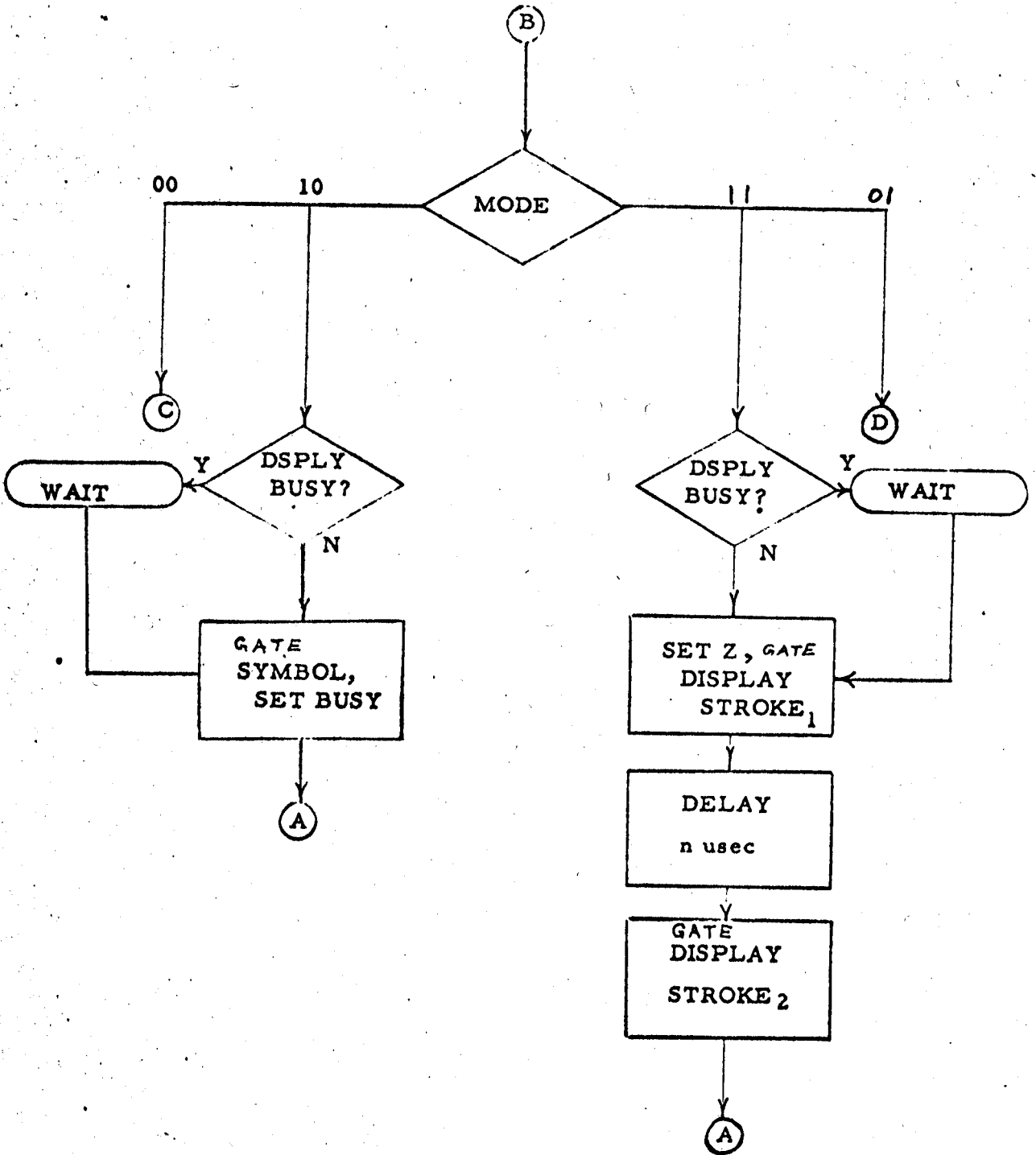


Fig. 7b

SYSTEM FLOW CHART

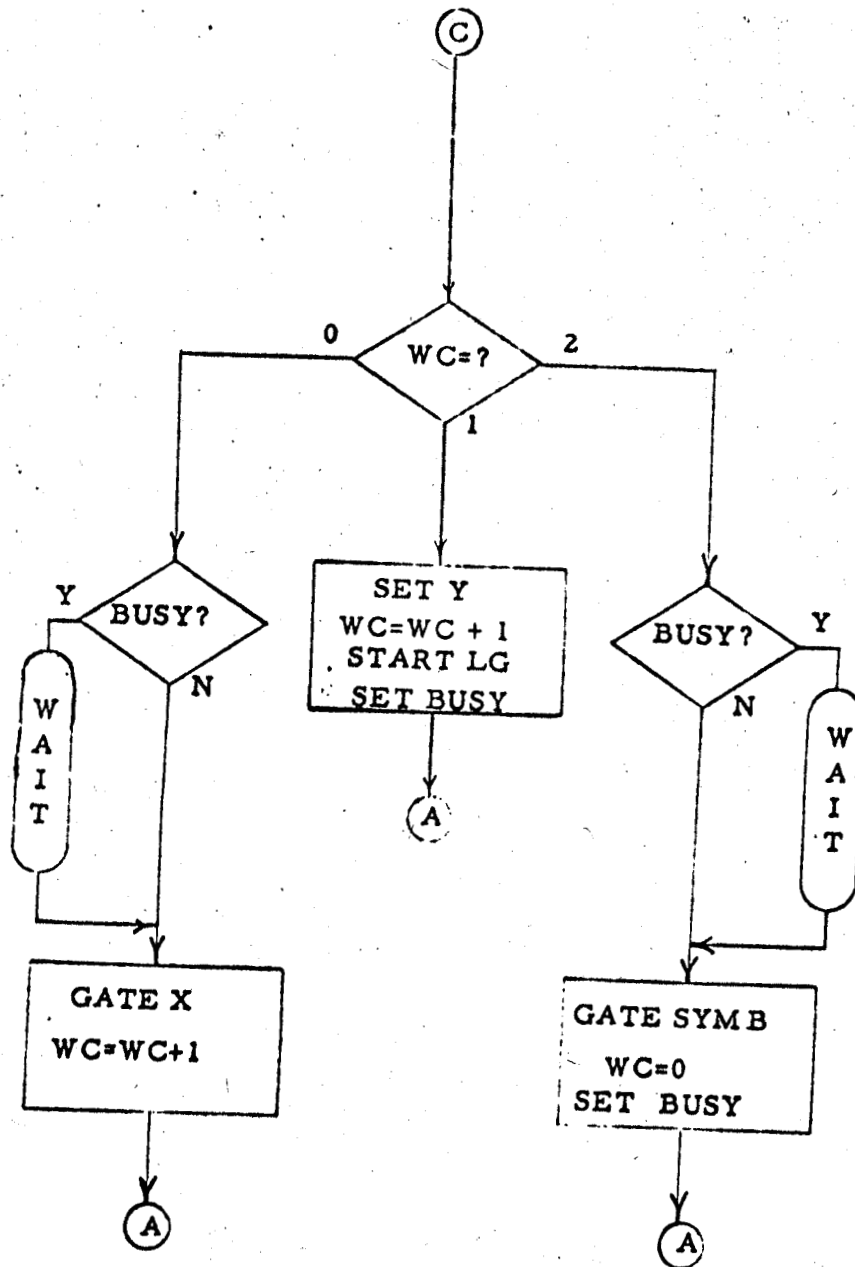


Fig. 7c

SYSTEM FLOW CHART

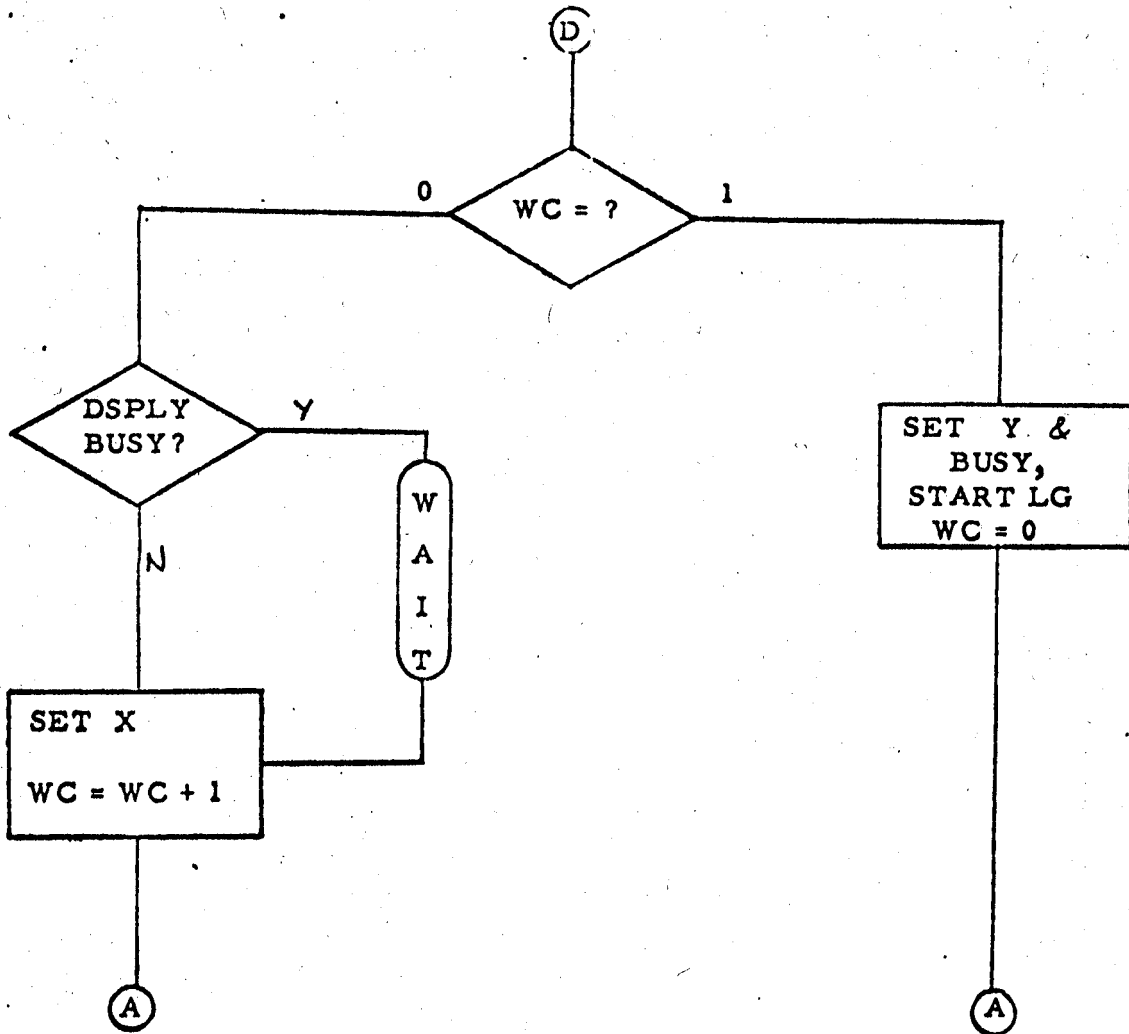


Fig. 7d

SYSTEM FLOW CHART

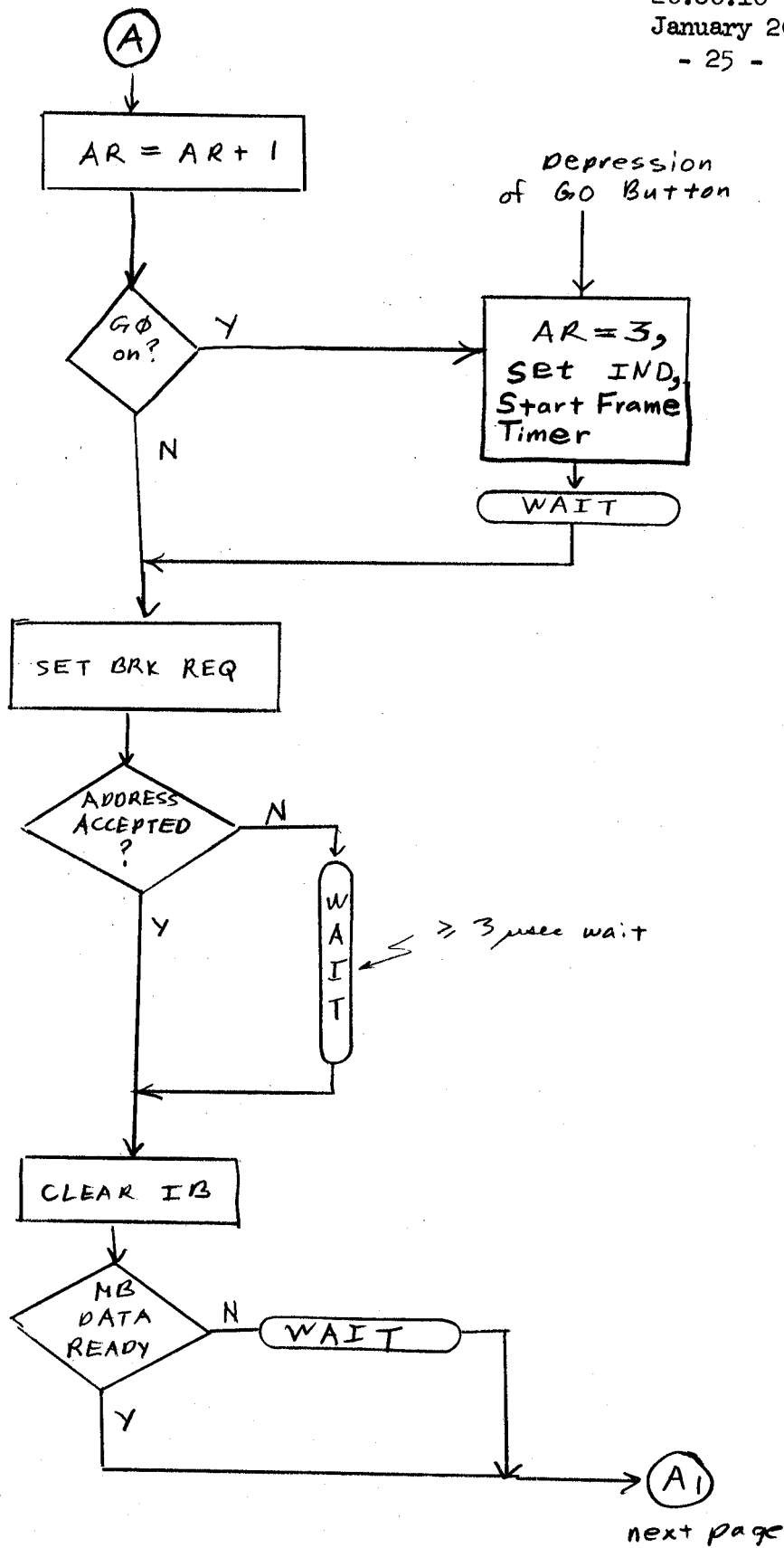


Fig. 7c SYSTEM FLOW CHART - Read Cycle, part 2.

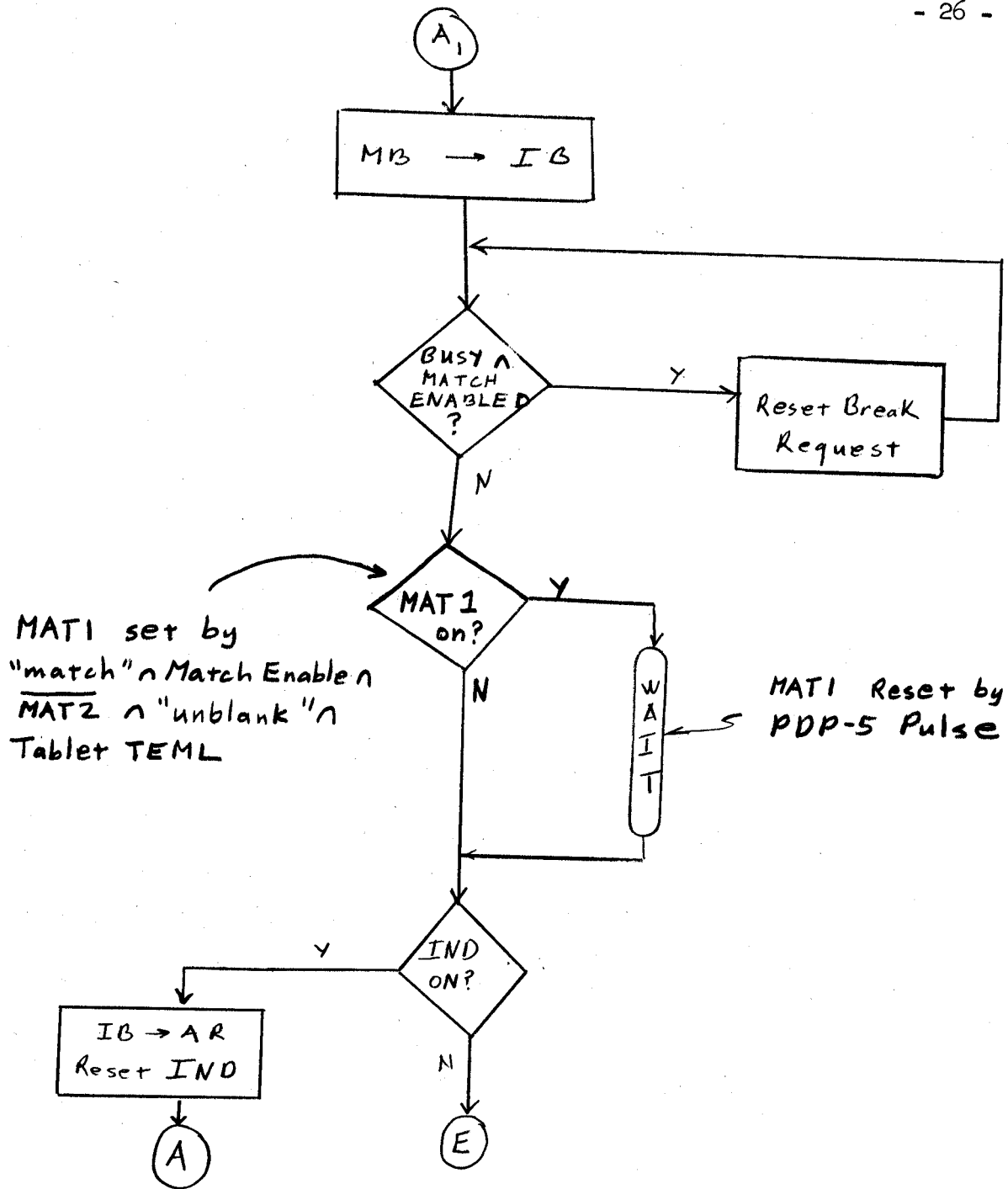


Fig. 7f SYSTEM FLOW CHART - Read Cycle, part 2.

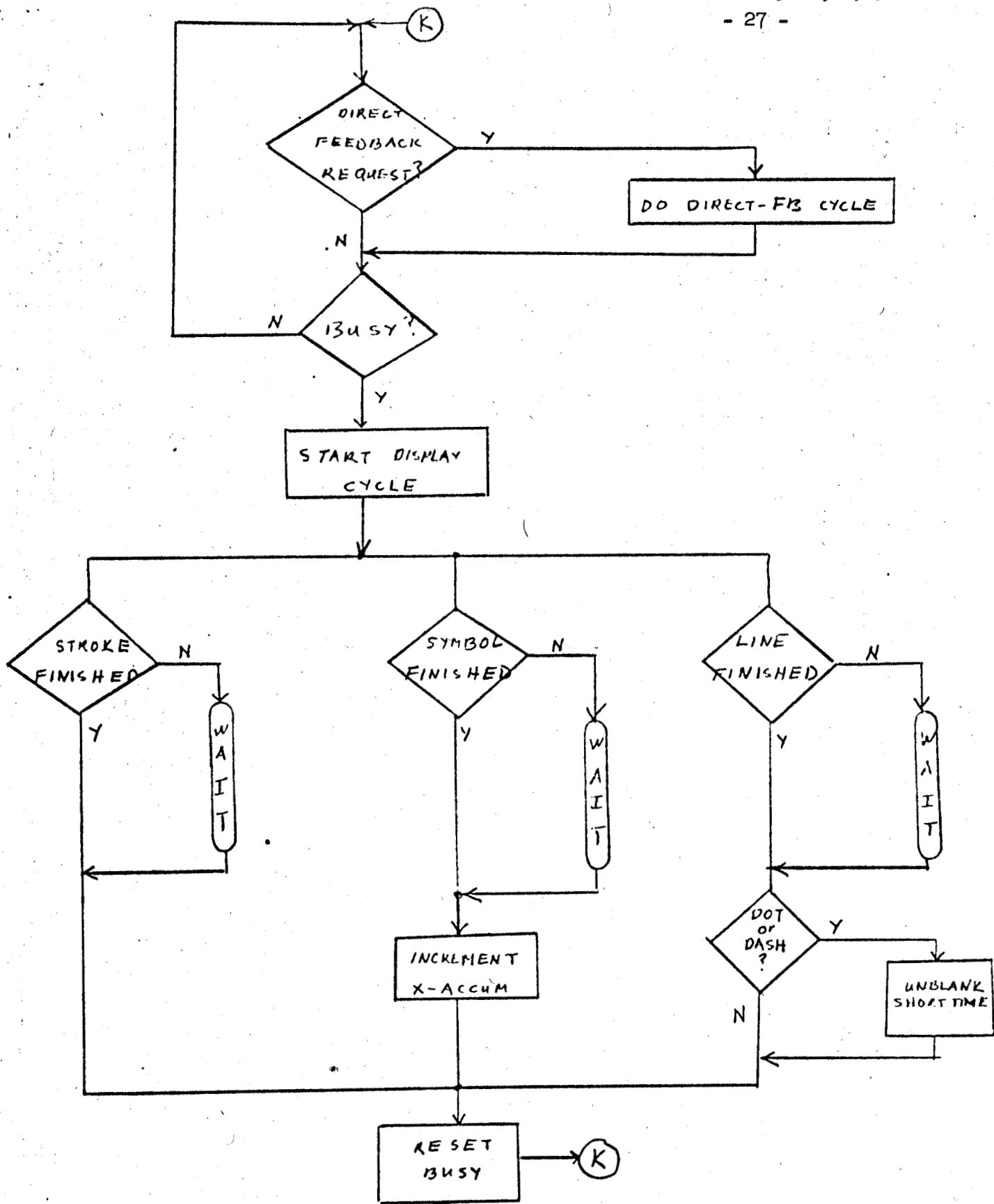


Fig. 7g SYSTEM FLOWCHART - Basic Display Cycle

PDP-5 - DISPLAY LOGIC INTERFACE

Figure 8 gives the lines that are sufficient to communicate with the PDP-5. The voltages given are all DEC standard levels and pulses. DEC manual C100, System Modules, describes all the DEC modules referred to in Figure 8, including loading rules. The appropriate level shifters are included in the Display Logic. A total of 60 cables, each capable of transmitting DEC standard signals, for the interconnection are considered part of the Display Logic and will allow the PDP-5 to be placed at least 10 feet from Display Logic. The plugs at the PDP-5 terminal are considered part of the PDP-5; plugs (for all 60 cables) at the Display Logic terminal will be supplied by Burroughs.

The PDP-5 Handbook, F-55 gives a description of the timing necessary to properly operate the Data Break system. The Gate Memory Buffer output pulse will occur 3 sec after the Address Accepted pulse in most cases (see Figure 10, pages 30 of F-55). It was mentioned above that the computer may Halt after issuing an Address Accepted, and then restart anytime thereafter (on the system clock) at the point indicated as 1 μ sec following the address accepted pulse (re. Figure 10).

Figure 8 PDP-5 interface Lines

PDP-5 To Display Logic

<u>Item</u>	<u>#Lines</u>	<u>Pulse/ Level</u>	<u>From Output of DEC Module type</u>	<u>True Voltage</u>	<u>False Voltage</u>	<u>Function</u>
(1)	12	L	1684 pin L*	0	-3	PDP-5 Memory Buffer Outputs
(2)	1	P	4603 pin F	+3	0	Address Accepted
(3)	1	P	4113 pin H	0	-3	Gate Memory Buffer Output
(4)	1	P	4605 pin E	-3	0	Reset GO ff, Start Display
(5)	1	P	4605 pin E	-3	0	Reset Match ff, Restart Display
(6)	1	P	4604 pin V	0	-3	1 mc Clock

Display Logic To PDP-5

			<u>Input To DEC Module type</u>			
(1)	12	L	4102 pin E**	0	-3	Display Address Reg. Outputs
(2)	1	L	4112 pin E	0	-3	Break Request
(3)	1	L	4102 pin E	0	-3	GO ff Output
(4)	1	L	4102 pin E	0	-3	Match ff Output

* The pin numbers given are representative only.

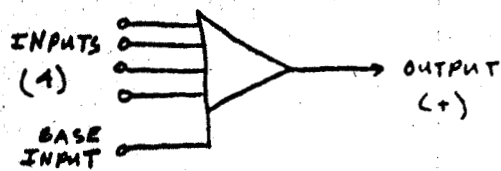
** The Display Address Register will be loaded by both the PDP-5 Memory Address register and Accumulator; both are type 4102 inputs.

RAND TABLET LOGIC

The basic building block for the RAND logic is the NOR circuit, which is symbolized by a triangle on the logic diagrams. This circuit can be connected to perform the LOGICAL AND, LOGICAL OR, INVERSION, and to construct TOGGLES. Logic levels for the circuits are 0 to -0.2 volts for the up signal and -4 to -6 volts for the down signal. True or false is either up or down according to the logic function being performed.

If the NOR circuit is performing the LOGICAL AND function, its output is true (down) only if all its inputs are true (up). If it is performing LOGICAL OR, its output is true (up) if any one of its inputs is true (down). Fan-in and Fan-out rules are a maximum of 4 in and 4 out. However, fan-in may be extended by ganging collectors with a common load register. Figures 9 and 10 give the circuit diagrams.

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ANY INPUT "-" → OUTPUT "+"

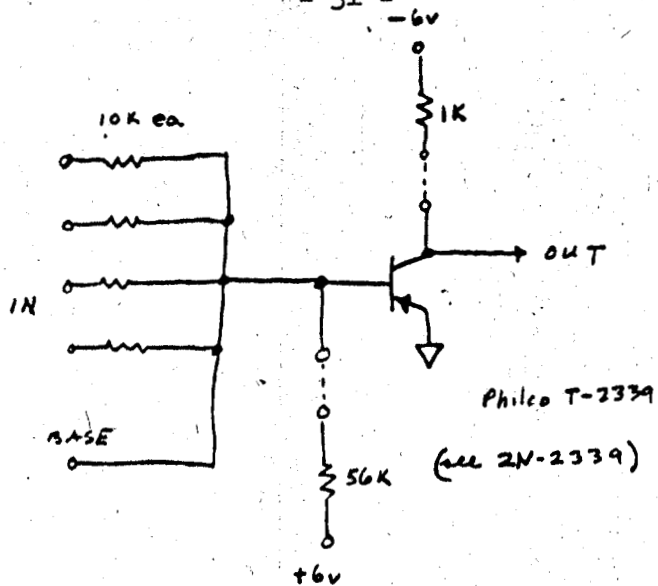
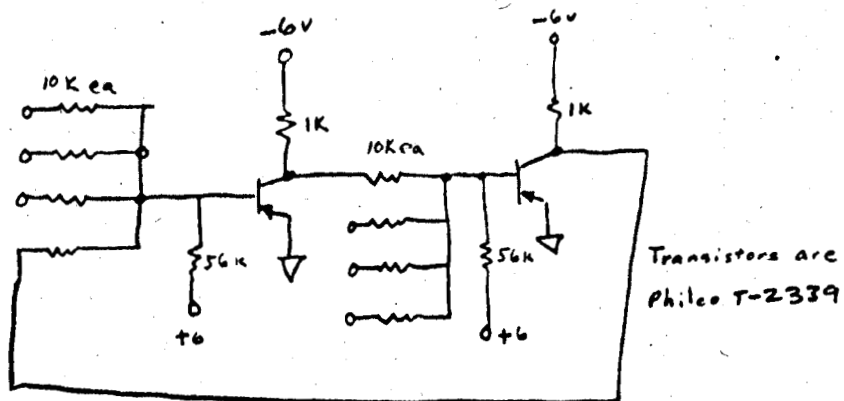
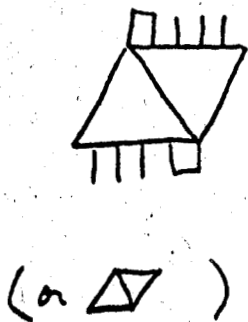


Figure 9 ... RAND NOR circuit.



Transistors are
Philco T-2339

Figure 10 ... RAND TOGGLE.

TABLET/DISPLAY LOGIC INTERFACE

The following lines will go between the Tablet Logic and Display Logic:

	<u># Lines</u>	<u>Level/Pulse</u>	<u>T/F Voltage</u>	<u>Function</u>
(1)	20	L	-6/0	tablet x and y coordinates (TXR and TYR)
(2)	1	L	-6/0	Enable Match, TXR and TYR VALID (TEML)
(3)	1	L	-6/0	Do direct feedback cycle. (DDFB)
(4)	1	P	-6/0	Direct feed-back cycle initiated

Only one line, (4), is necessary from the Display Logic to Tablet Logic, a pulse to signify that a Direct Feed-back Cycle has been initiated.

DDFB, (3), is sampled by the Display Logic at appropriate times (between symbols or lines), and if it is TRUE, the tablet coordinates, item (1), are to be gated directly to the major deflection D/A converters and a single spot is to be displayed at the tablet coordinate. DDFB will only be true if the tablet coordinates will be valid for 27* more microseconds, the display settling time for full screen deflection. Also, DDFB will only come true at approximately 5 ms. intervals (the clock is included in the RAND logic).

TEML is true anytime the tablet coordinates are valid for the purposes of a Match.**

Figure 11 is a logic diagram of the interface. The maximum loads on TXR and TYR are 2 (RAND) base loads, and on DDFB and TEML, 4 base loads.

* This could be 0, 9, 18, 27, or 36; the smallest that is sufficient.

** The Match toggle which interrupts the PDP-5 is set by $TEML \wedge \text{Enable Match} \wedge \text{"coordinate match occurs"} \wedge Z - \text{unblank} \wedge \text{"no previous match has occurred in this frame."}$

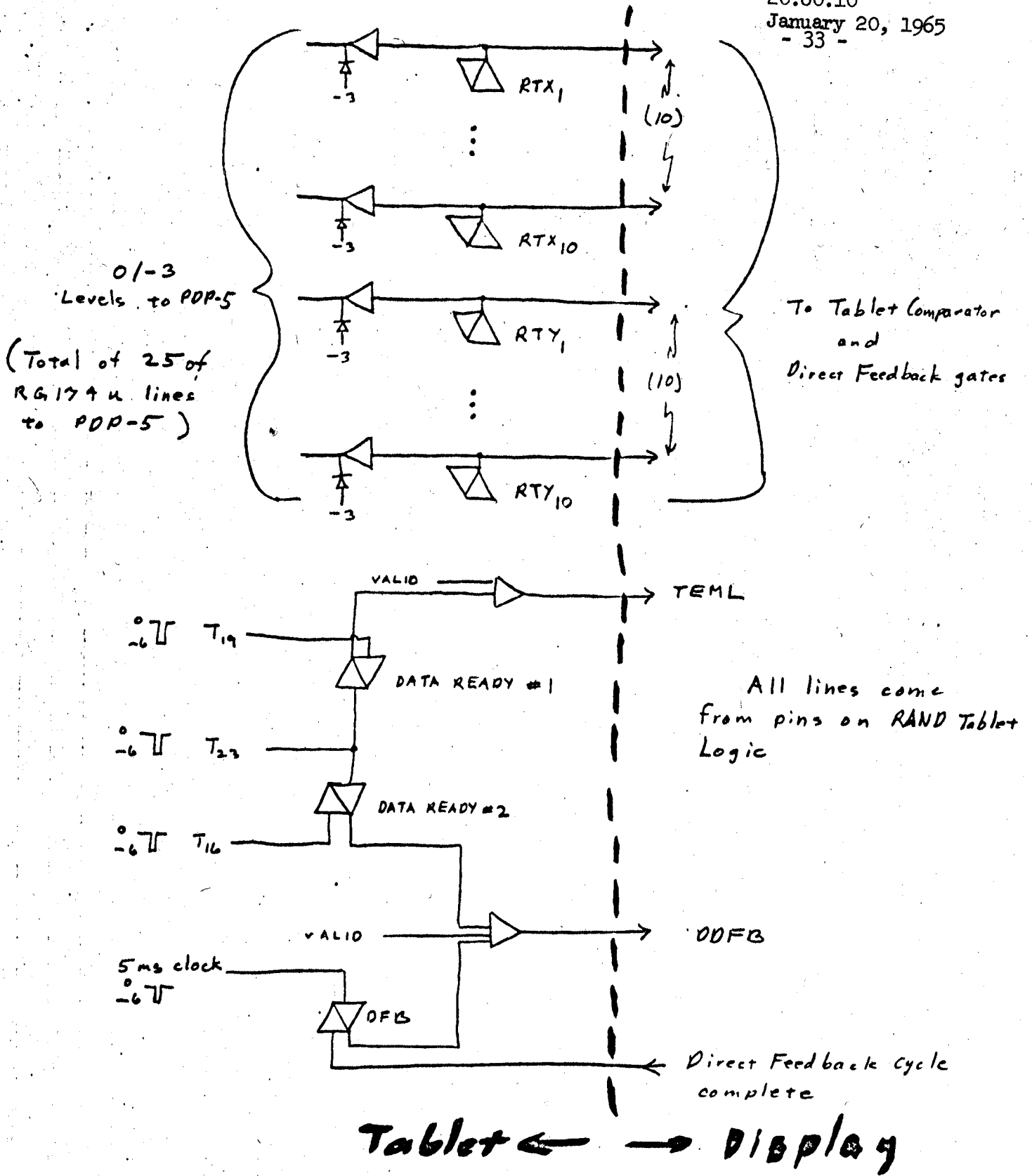


Fig. 11 Tablet / Display Interface

RAND TABLET LOGIC INSTALLATION

Provision (i.e., mounting holes) shall be provided in the Display Logic cabinet for installation (by UCB after delivery) of 2 RAND Logic cages. One cage, to which the Tablet/Tablet Logic cables and Tablet Logic/Display Logic lines attach is a standard 19" ELCO cage, the second is a similar but $\frac{1}{2}$ length ELCO cage to which the PDP-5/Tablet Logic lines attach (see Figure 12).

The 2 cages should be adjacent, but the mounting may be by standard relay-rack mount end-brackets on the cages, or by a flat end-plate as shown in Figure 13. The shortened- $\frac{1}{2}$ cage may be any length from 6" to 19", whatever is convenient within the console. The cards and wiring should be accessible and in the forced air-flow path of the Display Logic. Figure 13 shows an end-view of a RAND/ELCO cage.

A path will also be provided for the Tablet/Tablet Logic cables - 40 ea. RG 174U and 1 ea. $\frac{1}{4}$ " bundle consuming an approximately 1" diameter circular area. These cables will run from the RAND Logic cages to the Tablet Cable Hole, a hole at a convenient spot to the right side and in-line with the RAND tablet. Figure 14 is a sketch of the console with the important features dimensioned. Figure 15 gives the RAND Tablet dimensions.

The 60 cables mentioned above (PDP-5 Display Logic Interface, page 26) include the 28 cables necessary for connecting the Tablet Logic directly to the PDP-5.

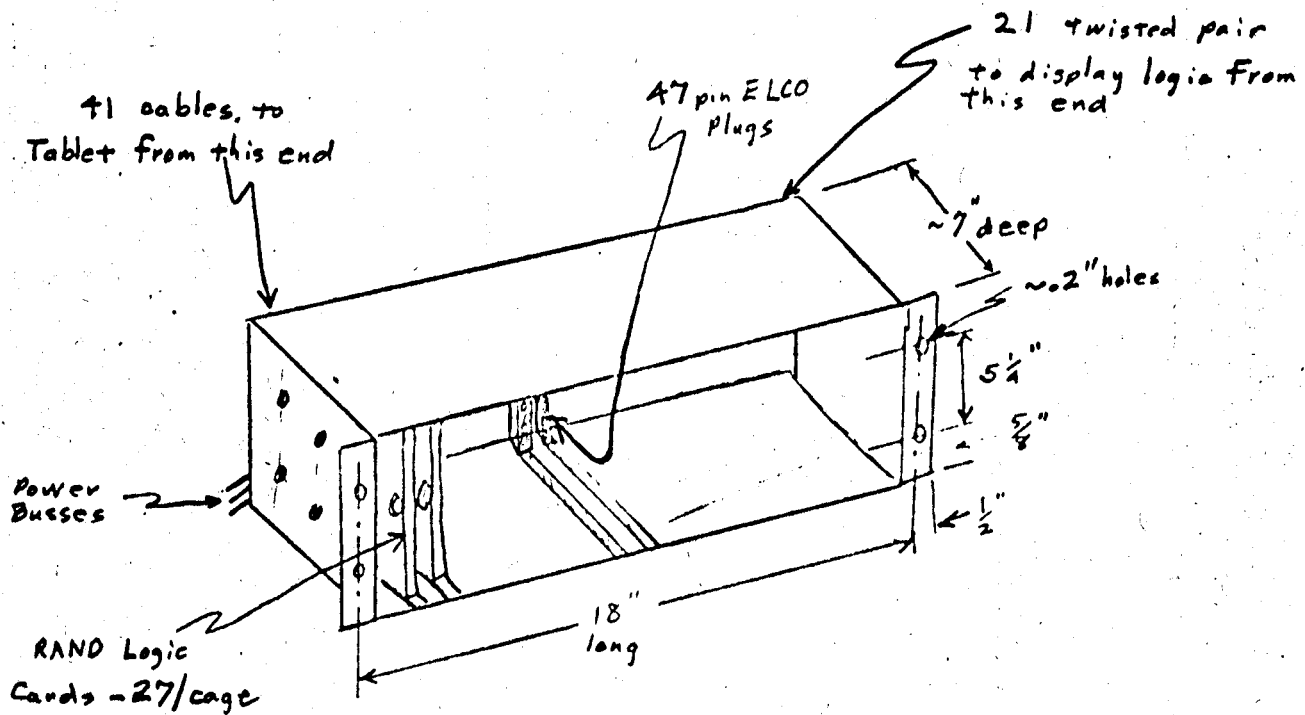


Fig. 12 - 19" ELCO cage with standard relay rack mounting end plates shown. Shortened cage is at least 6" long.

Note: Cage assembled from Elco Corporation parts:

- (a) "Varipac" Guideplates MOD # 53-9016-1302
- (b) "Varipac" Guides for 1/16" cards, 5" long with retainers, MOD # 53-9016-1204
- (c) Printed circuit connectors Ser # 7001, 47 pin, etc. code # 7001-47-525

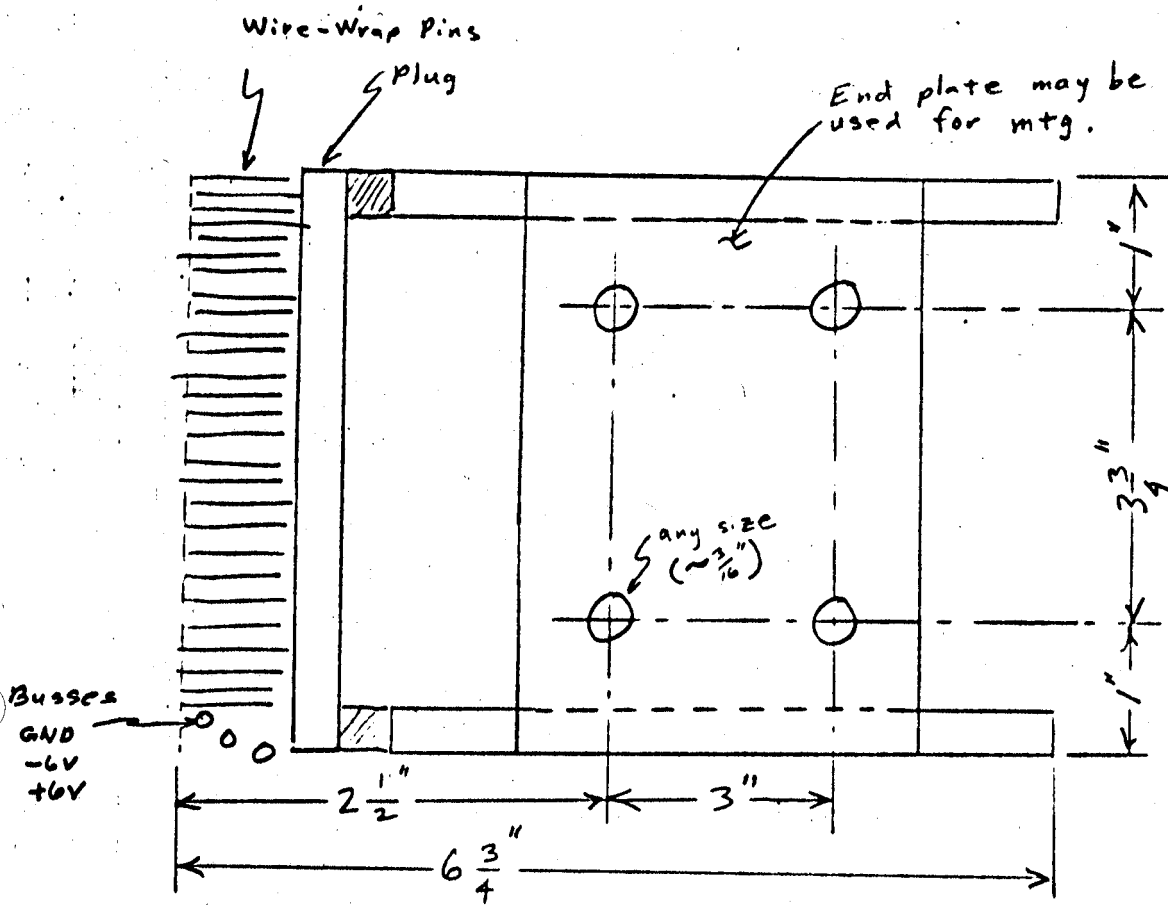
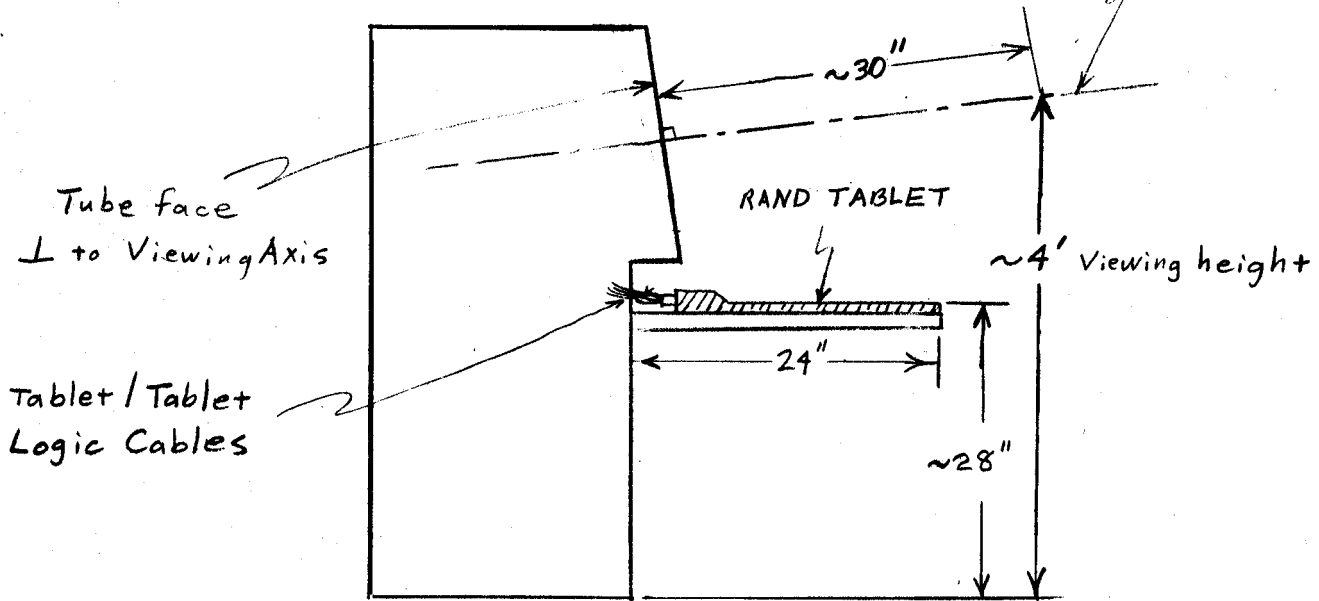


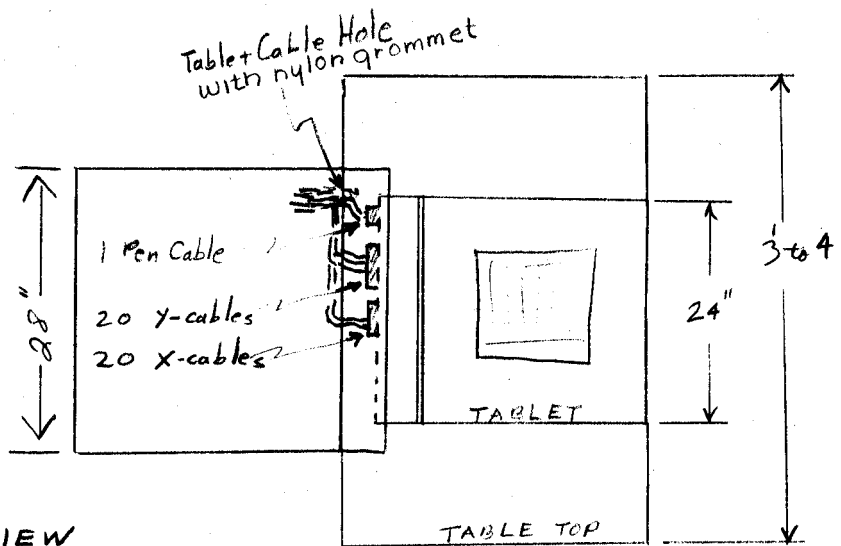
Figure 13. End View of ELCO Cage with End-Plate dimensions shown. (not to scale)

Axis of tube and
Viewing axis



SIDE VIEW

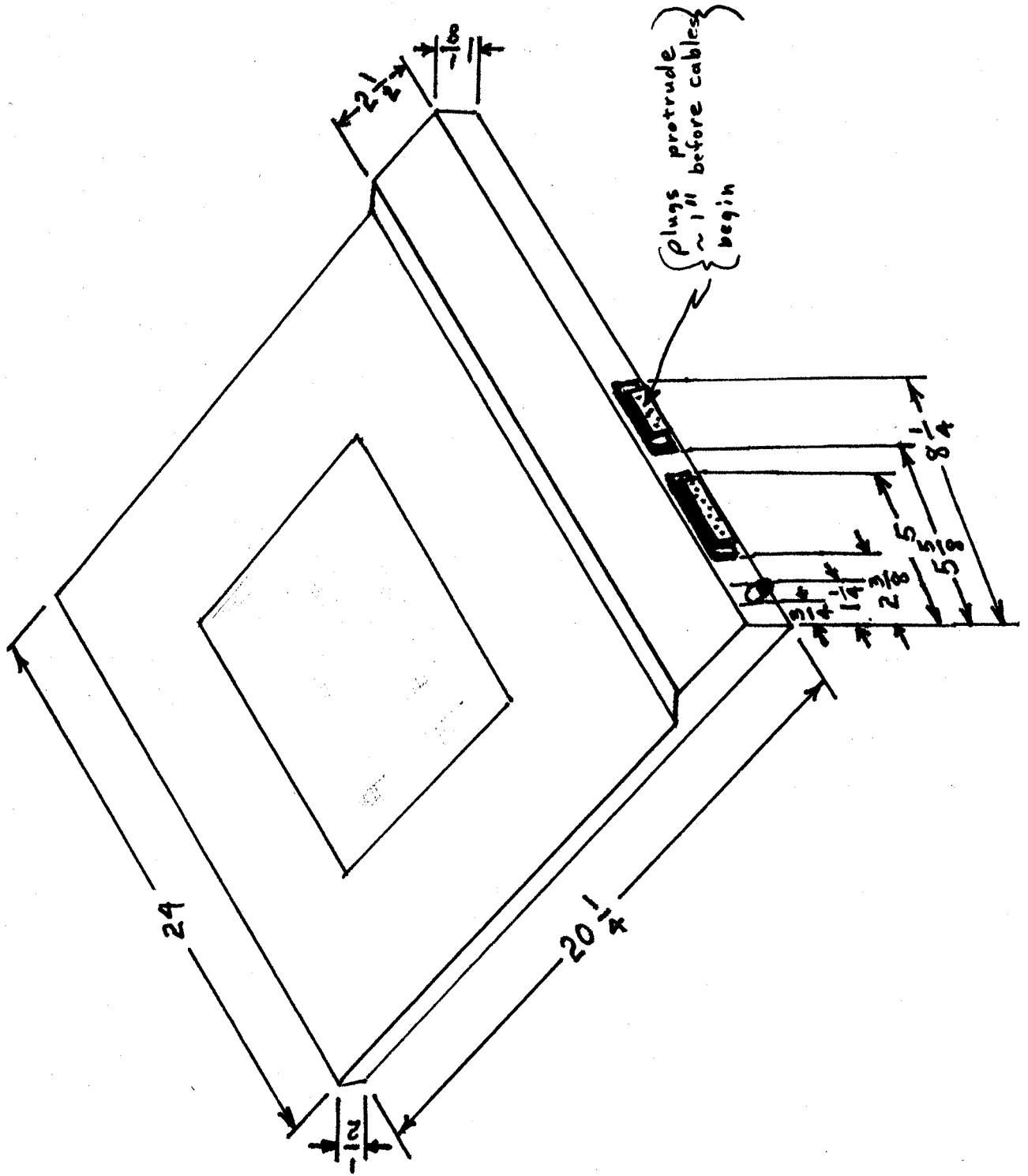
Note: Only buttons showing on outside of console are POWER, G₀, and Intensity. Table is removable.



TOP VIEW

Figure 14 Display Console Configuration

Figure 15 RAND Tablet Dimensions



POWER FOR RAND TABLET LOGIC

The following amounts of DC power will be provided for the tablet logic. This should be switched on and off the same as the display logic with the restriction that all dc voltages be turned on simultaneously, or in the order +6, -6, +40.

Current Actually Used (amps)	Voltage dc (volts)	Maximum Ripple (mv RMS)	Load Regulation (Load Change 5-100%) (mv)
3	-6	2	5
0.3	+6	2	5
0.1	+40	2	5

ACCEPTANCE TESTS

Acceptance Test shall verify the following items. Exact test procedure will be mutually agreed upon later. Tests will not be performed in sync with 60 cps line voltage but at such a different frequency to make apparent any placement errors due to this source of error.

1. In Normal brightness demonstrate 100:1 constant brightness lines, 4 types

2:1 constant brightness symbols (128 symbols per line and 64 symbols per line).

4 sizes of script at constant brightness. A script pattern exhibiting closed and open figures of duration sufficient to prove the accuracy and stability of the script generator will be used.

Formatted characters with offsets.

Specified resolution

2. Line, Script, and Symbols in three distinguishable brightness levels.
3. Demonstrate 1000:1 lines (constant brightness over 100:1).
4. Demonstrate operation of Match Comparator.
5. Demonstrate satisfactory operation of the PDP-5/Display Logic Interface.

Burroughs Corporation

APPENDIX A

LINE GENERATOR OPERATION

The Burroughs LB 10B line generator causes deflection signals in the X and Y axes to be synchronously generated, which results in the CRT beam tracing out a continuous straight line path. The Z axis or intensity is modulated during this period by a waveform determined by a digital command. The beginning and termination of the line segments are specified digitally and these end points are also the basic positioning circuitry of the display system. A block diagram illustrating the technique used is shown in Figure A-1.

The LG 10B line generator may construct lines in any direction specified by the two end points, (X_0, Y_0) and (X_1, Y_1) . These two end points are fed both to the X and Y dual digital analog converters and the constant rate generator. The constant rate generator controls the ramp generator as a function of delta X and delta Y so that the elapsed time between the beginning and end of the ramp is proportionally shorter for short segments. The X and Y dual digital-to-analog converters then operate with the ramp generator and position inputs to produce the X and Y deflection signals.

The lines are drawn at a constant writing rate so that both long and short lines appear at the same intensity to the observer.

The exact requirements for identical X and Y ramp is satisfied by using the same ramp as the reference voltage input to all of the D/A converters, both X and Y. Therefore, since the output voltages are the sum of products of a constant, times an identical voltage variation, identical ramp shaping in X and Y and identical starting times are assured.

The content of the X and Y accumulator at the start of a line segment is that which was left as a result of the previous instruction. At the end of the line segment drawing time, the contents of the X and Y holding registers are transferred to the X and Y accumulators so that the end of one line segment may be the beginning of the next.

Burroughs Corporation

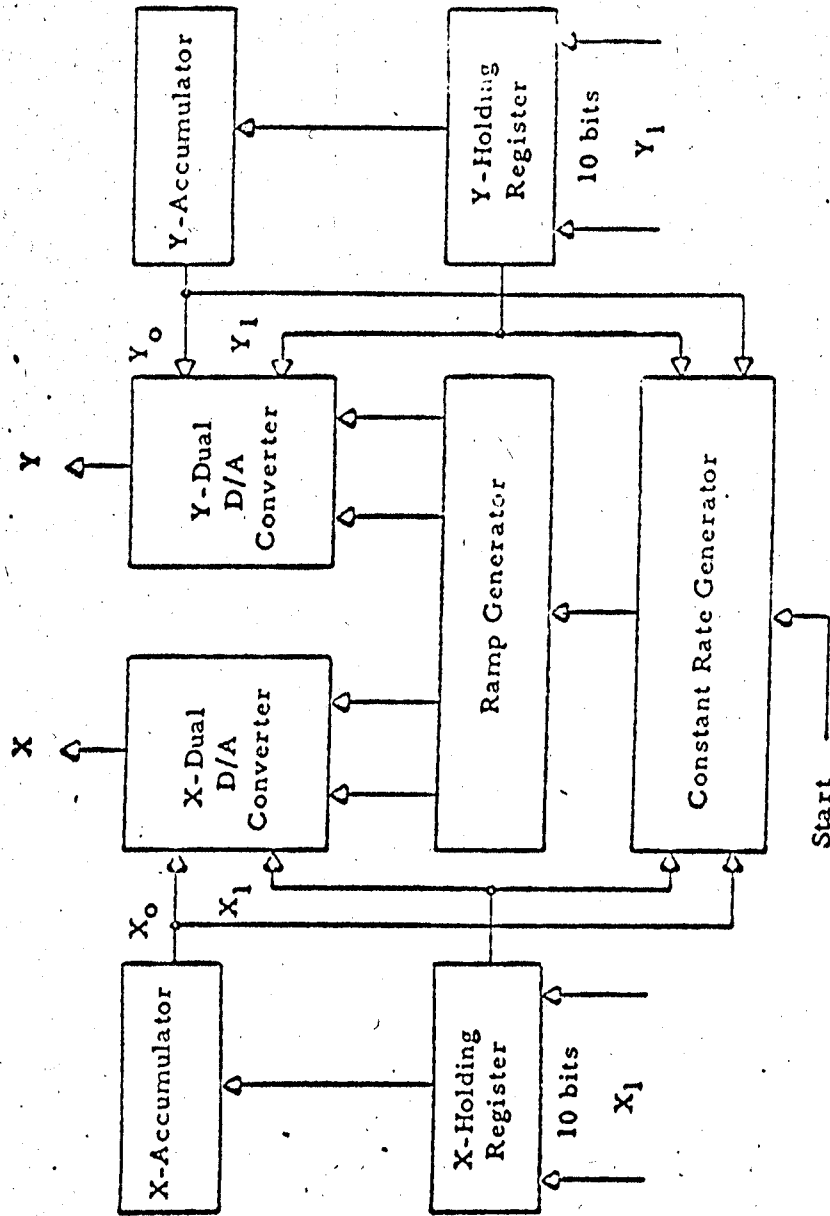


Figure A-1 LG 10 Line Generator - Block Diagram

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TABLE I
SYMBOL GENERATOR CHARACTERISTICS

INPUTS	Character (symbol) select code	64 character	128 character
		Size Code	6 bits
Matrix Strobe (pulse)		2 bits	2 bits
Voltage Range: X, Y		1.0 usec	1.0 usec
Z		+ 2 volts	+ 2 volts
		+ 3 volts	+ 3 volts
POWER		100 watts	120 watts
SPEED	"Set up" (may be used for positioning)	3 to 10 usec	3 to 10 usec
Maximum time - (20 segments, depends on model)			
Model A	Model B	Model C	Operation
500 to 30 usec	30 to 16 usec	—————	Asynchronous*
—————	16.8 to 10.5 usec	8.4 to 2.1 usec	Synchronous
* Average alphanumeric time - depends on model but is usually maximum time divided by 1.5			

METHOD OF OPERATION

The symbol generator performs three primary functions: first, the symbol command word is accepted and decoded; second, based on the selected symbol, command information for drawing the symbol is read out of a special memory; and third, this command information is used to construct X, Y, and Z (unblanking) waveforms to drive the CRT display.

The symbols are formed from a series of straight-line segments. Each segment is connected to the previous segment, but can be individually oriented through 25 combinations of slope and length. In addition, the intensity of each segment may be controlled on or off.

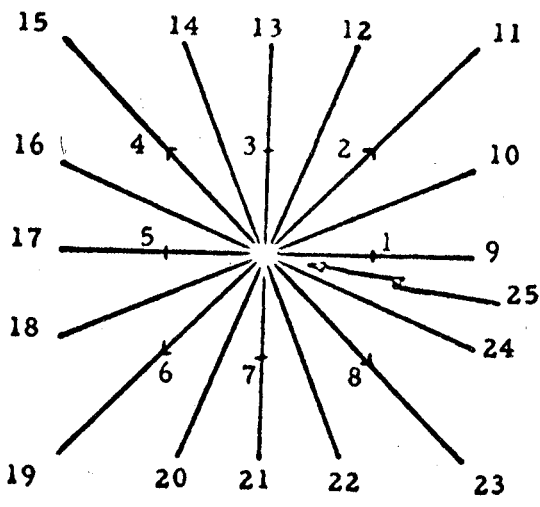
The structure of the individual segments and a typical character is diagrammed in Figure 1. A typical character set of alphanumeric and special characters is shown in Figure 2. The method is efficient, both in terms of encoding the information required to generate a character in a minimum number of commands (i. e., the slope, length and intensity of each segment), and in terms of the intrinsic brightness capability (since for a very high percentage of the allowable generation time, the entire beam current is exciting the phosphor).

The symbol generator decoding array samples and stores the character command. The resulting bit combination is then used to select and energize line drivers. The line drivers then "set up" the core memory with the information required to generate the selected characters. The selected character is then read out of the core memory by time sequenced resetting of the individual core columns. The information gained from each column defines a character stroke as to length and direction. The outputs are combined in analog integrator circuits to produce the composite positioning video describing the symbol.

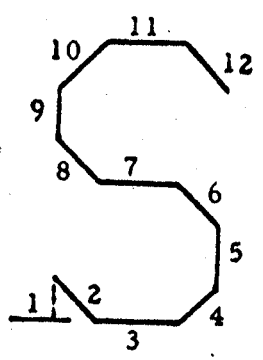
The core also contains the data necessary to control the blanking, or Z-axis, for the characters. This data is sequenced out with the stroke information.

Size control (four sizes) is accomplished by decoding two size control bits to electronically switch attenuators. The resistance ratios of the attenuators are directly proportional to the desired symbol size ratios and are independent of each other.

Pictures of both the synchronous and asynchronous models are shown in Figures 3 and 4.



a) Line Segment Combinations



b) Typical Character Construction

Figure 1 Line Segment and Character Structure

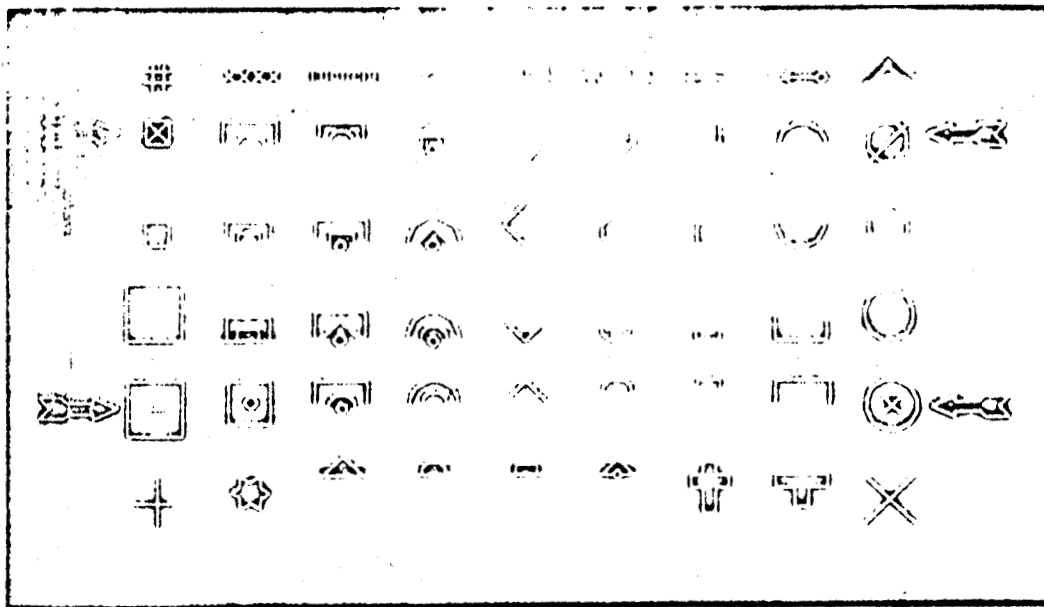
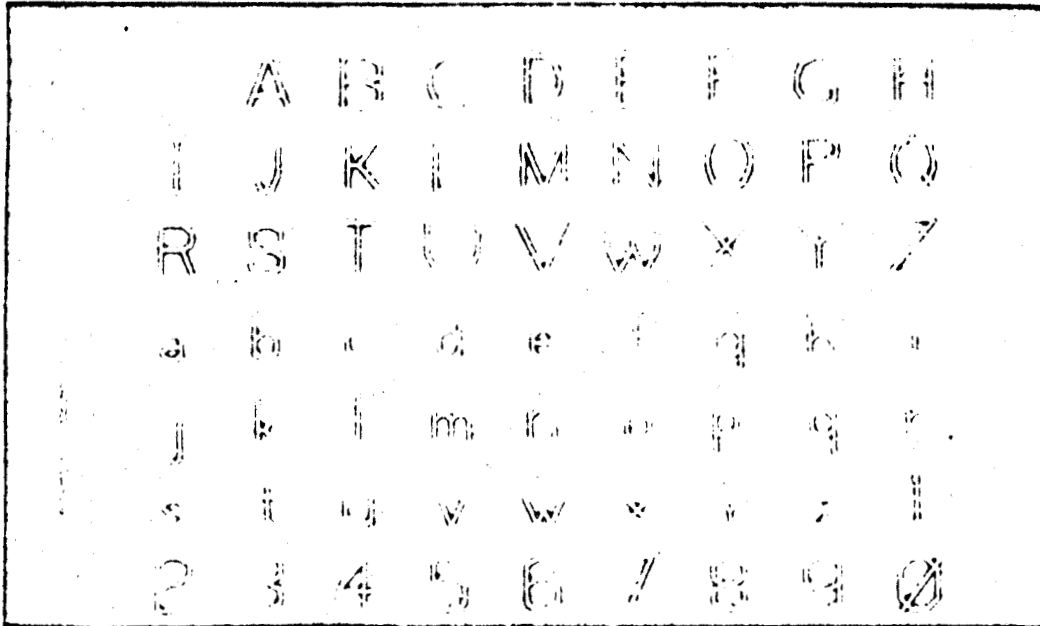
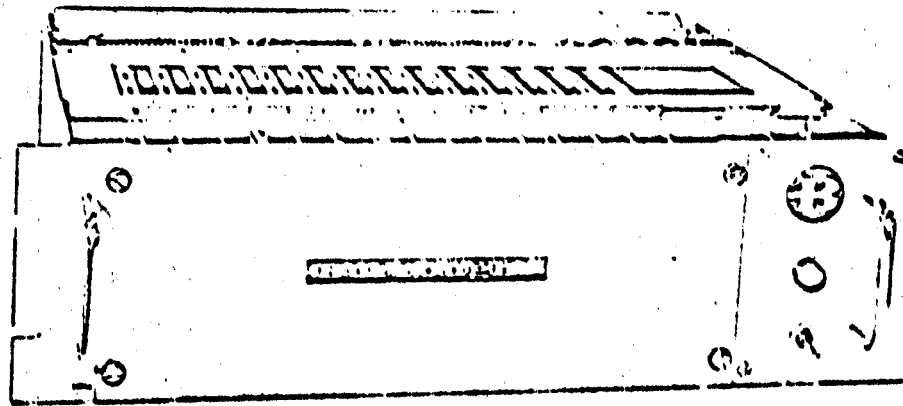
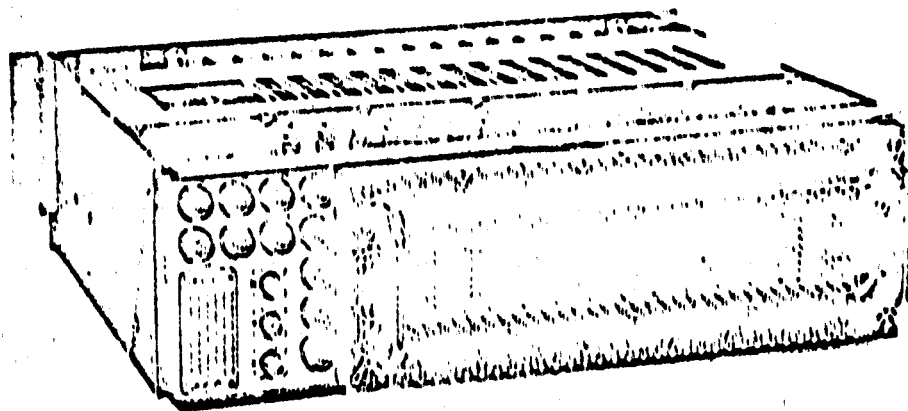


Figure 2 Typical Character Set of Alphanumeric
and Special Symbols



a) Front View

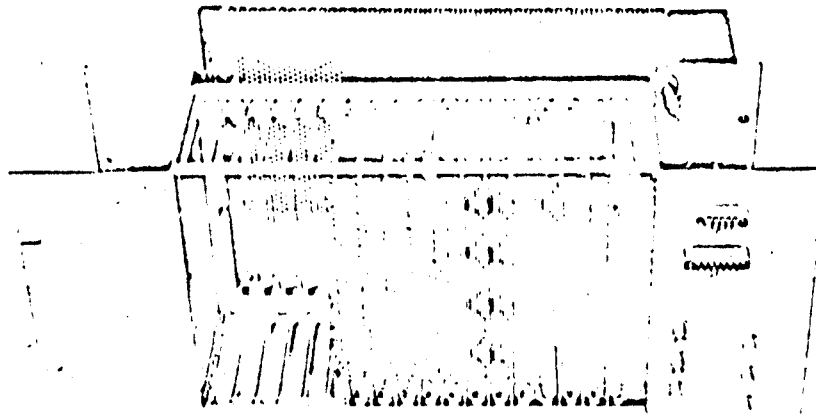


b) Rear View

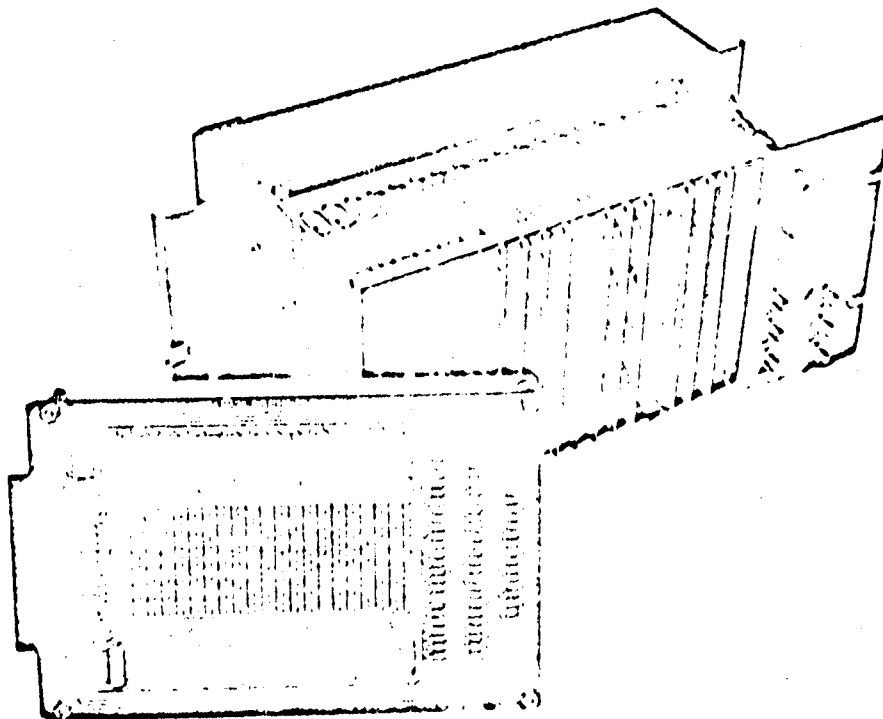
Figure 3 Asynchronous Symbol Generator

b-6

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RETRIEVAL SYSTEM.



a) Front View



b) Front View With Core Board

Figure 4 Synchronous Symbol Generator